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Remarks

This amendment is responsive to the Office Action of October 24, 2006. Reexamination and reconsideration of claims 1-44 is respectfully requested.

Summary of The Office Action

Claims 1, 3, 5-16, and 29-34 were rejected under 35 U.S.C. §103(a) as being unpatentable over Long et al. (US Pat. No. 6,393,545)(Long) in view of McKenzie (US Pat No. 6,453,398)(McKenzie).

Claims 17-19, 21-25, 28, 37-38 and 41-44 were rejected under 35 U.S.C. §103(a) as being unpatentable over Long, in view of McKenzie, and further in view of Leung et al. (US PG Pub. No. 20050044467)(Leung).

Claims 35-36 were rejected under 35 U.S.C. 103(a) as being unpatentable over Long, in view of McKenzie, and further in view of Korhonen (US Pat. No. 6,742,148)(Korhonen).

Claims 26-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Long, McKenzie, Leung, and Nakamura (US Pat. No. 6,523,135)(Nakamura).

Claims 2 and 40 were rejected under 35 U.S.C. 103(a) as being unpatentable over Long, in view of McKenzie, and further in view of Idleman et al. (US Pat. No. 5,274,645)(Idleman).

Claims 4, 20 and 39 were rejected under 35 U.S.C. 103(a) as being unpatentable over Long, McKenzie, Leung, and Chauvel et al. (US PGPub. No. 20040024970)(Chauvel).

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Argument

Claims 1, 3, 5-16, and 29-34 were rejected under 35 U.S.C. §103(a) as being unpatentable over Long in view of McKenzie. Long is used by the Office Action to assert that a memory mapping logic is disclosed. The "memory mapping logic" in Long is a conventional virtual to physical memory mapping unit. McKenzie is used by the Office Action to assert that a memory quality assurance logic is disclosed. The "memory quality assurance logic" in McKenzie processes complete pages. Thus, claim 1, and all the independent claims have been amended to include the additional limitation that the "memory locations" claimed are less than a page in size. Support for this limitation appeared in original paragraphs [0072] and [0073], which have also been amended to remove page sized operations. This amendment removes McKenzie as prior art, leaving all the independent claims, and thus all the dependent claims as well, not obvious and in condition for allowance.

Claim 1

Claim 1 has been amended to include the additional limitation that the "memory locations" claimed are less than a page in size. Support for this limitation appeared in original paragraphs [0072] and [0073], which have also been amended to remove page sized operations. Since McKenzie only discloses page sized actions, claim 1 is not obvious and is in condition for allowance.

Claim 5

This claim depends from claim 1, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the memory quality assurance logic is configured to selectively logically remove a memory location from a first set of memory based on a memory testing result. The Office Action asserts that Long discloses this element. The Office Action relies on Long, col. 1, lines 47-51 to support this assertion. However, these lines describe actions associated with cache miss processing. The "invalidating" described in Long deals with the freshness of a cache value and a cache value replacement policy. It has nothing to do with reconfiguring a memory mapping logic to logically remove a memory location from a set of memory. While the contents of a cache line may be evicted, the cache line

remains available for other values. In the claim, the memory location becomes unavailable. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 6

This claim depends from claim 1, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the memory quality assurance logic is configured to selectively logically replace a memory location with its temporary mirroring memory location based on a memory testing result. The Office Action asserts that Long discloses this element. The Office Action relies on Long, col. 1, lines 45-46 and lines 47-51 to support this assertion. However, these lines describe actions associated with cache miss processing. The "replacing" described in Long deals with moving cache values in and out of a cache. It has nothing to do with reconfiguring a memory mapping logic to logically replace a memory location in a set of memory. While the contents of a cache line may be moved, the cache line remains available for other values. In the claim, the memory location becomes unavailable. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 7

This claim depends from claim 1, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the memory quality assurance logic is configured to selectively logically replace a memory location with a different memory location based on a memory testing result. The Office Action asserts that Long discloses this element. The Office Action relies on Long, col. 1, lines 45-46 and lines 47-51 to support this assertion. However, these lines describe actions associated with cache miss processing. The "replacing" described in Long deals with moving cache values in and out of a cache. It has nothing to do with reconfiguring a memory mapping logic to logically replace a memory location in a set of memory. While the contents of a cache line may be moved, the cache line remains available for other values. In the claim, the memory location becomes unavailable. For this additional reason this claim is not obvious and is in condition for allowance.

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Claim 11

This claim depends from claim 1, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the memory quality assurance logic includes data stores for storing freshness, quality, relationship, and/or reconfiguration data. The Office Action asserts that McKenzie discloses this element. The Office Action relies on McKenzie, col. 6, lines 10-13 to support this assertion. However, these lines describe storing status information (e.g., whether test finished) or error information. Neither of these are freshness, quality, relationship, or reconfiguration information. Freshness data is described as concerning how recently a memory location has been accessed and/or error checked. Quality data is described as concerning error rates, error types, and so on. Clearly neither status information nor error code information disclose either freshness or quality data. Furthermore, the reference does not show the storage location as being in the memory quality assurance logic. For these additional reasons this claim is not obvious and is in condition for allowance.

Claim 12

This claim depends from claim 1, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the memory quality assurance logic is operably connected to data stores for storing freshness, quality, relationship, and/or reconfiguration data. The Office Action asserts that McKenzie discloses this element. However the Office Action also asserted that McKenzie disclosed the data stores as being in the memory quality assurance logic. Thus, the Office Action is internally inconsistent concerning claims 11 and 12. Furthermore, the reference describes storing status information (e.g., whether test finished) or error information, which does not teach string freshness, quality, relationship, or reconfiguration information. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 13

This claim depends from claim 1, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the second memory location is in internal memory of the memory mapping logic. The Office Action asserts that McKenzie discloses this element. The Office Action relies on McKenzie, col. 3, lines 6-9 to support this

assertion. However, these lines and indeed all of McKenzie show separate pages of memory being accessed by external logics. None of McKenzie shows the second memory location being internal to the mapping logic, it only shows memory separate from the mapping logic. Separate memory is not memory internal to a memory mapping logic. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 14

This claim depends from claim 1, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the second memory location is in internal memory of the memory quality assurance logic. Once again the Office Action asserts that McKenzie discloses this element. The Office Action once again relies on McKenzie, col. 3, lines 6-9 to support this assertion. The Office Action is internally inconsistent because in one rejection it asserts the memory is internal to the memory mapping logic while in another rejection it uses the same citation to assert that the memory is internal to the quality assurance logic. The Office Action must decide whether the purportedly internal memory is internal to the purported memory mapping logic or the purported memory quality assurance logic. In either case, the Office Action still has it wrong. The cited lines and indeed all of McKenzie show separate pages of memory being accessed by external logics. None of McKenzie shows the second memory location being internal to the quality assurance logic, it only shows memory separate from the quality assurance logic. Separate memory is not memory internal to a memory quality assurance logic. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 29

Claim 29 has been amended to include the additional limitation that the "memory locations" claimed are less than a page in size. Support for this limitation appeared in original paragraphs [0072] and [0073], which have also been amended to remove page sized operations. Since McKenzie only discloses page sized actions, claim 1 is not obvious and is in condition for allowance.

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Claim 32

This claim depends from claim 29, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the memory quality assurance logic includes data stores for storing freshness, quality, relationship, and/or reconfiguration data. The Office Action asserts that McKenzie discloses this element. The Office Action relies on McKenzie, col. 6, lines 10-13 to support this assertion. However, these lines describe storing status information (e.g., whether test finished) or error information. Neither of these are freshness, quality, relationship, or reconfiguration information. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 33

This claim depends from claim 29, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the memory quality assurance logic is operably connected to data stores for storing freshness, quality, relationship, and/or reconfiguration data. The Office Action asserts that McKenzie discloses this element. However the Office Action also asserted that McKenzie disclosed the data stores as being in the memory quality assurance logic. Thus, the Office Action is internally inconsistent concerning claims 32 and 33. Furthermore, the reference describes storing status information (e.g., whether test finished) or error information. Neither of these are freshness, quality, relationship, or reconfiguration information. For these additional reasons this claim is not obvious and is in condition for allowance.

Claims 17-19, 21-25, 28, 37-38 and 41-44 were rejected under 35 U.S.C. §103(a) as being unpatentable over Long, in view of McKenzie, and further in view of Leung.

Claim 17

Claim 17 has been amended to include the additional limitation that the "memory locations" claimed are less than a page in size. Support for this limitation appeared in original paragraphs [0072] and [0073], which have also been amended to remove page sized operations. Since McKenzie only discloses page sized actions, claim 17 is not obvious and is in condition for allowance.

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Claim 22

This claim depends from claim 17, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites selectively logically removing a memory location from a first set of memory. The Office Action asserts that Long discloses this element. The Office Action relies on Long, col. 1, lines 45-51 to support this assertion. However, these lines describe actions associated with cache miss processing. The "removing" described in Long deals with moving a value out of a cache. It has nothing to do with reconfiguring a memory mapping logic to logically remove a memory location from a set of memory. While the contents of a cache line may be evicted, the cache line remains available for other values. In the claim, the memory location becomes unavailable. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 23

This claim depends from claim 17, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites selectively logically replacing a memory location with a third memory location. The Office Action asserts that Long and McKenzie disclose this element. The Office Action relies on Long, col. 1, lines 45-51 and McKenzie col. 3, lines 6-9, and figure 1, items 110-116 to support this assertion. However, these lines describe actions associated with cache miss processing. Furthermore, these lines, and indeed all the references, deal only with "pairs" of memory (e.g., location to test, mirror location). None of the references describe replacing a tested location with a third location. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 25

This claim depends from claim 17, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites storing a quality data that is based on testing of a memory location. The Office Action asserts that McKenzie discloses this element because it stores a status value (e.g., test finished) or an error data. Neither a status code nor an error code are a "quality" data as claimed and defined. Consider paragraph [0033] of the

specification which describes quality data as concerning an error rate and/or an error type. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 37

Claim 37 has been amended to include the additional limitation that the "testable memory location" claimed is less than a page of memory. Support for this limitation appeared in original paragraphs [0072] and [0073], which have also been amended to remove page sized operations. Since McKenzie only discloses page sized actions, claim 37 is not obvious and is in condition for allowance.

Claim 38

Claim 38 has been amended to include the additional limitation that the "target memory location" and the "replacement memory location" are less than a page of memory. Support for these limitations appeared in original paragraphs [0072] and [0073], which have also been amended to remove page sized operations. Since McKenzie only discloses page sized actions, claim 38 is not obvious and is in condition for allowance.

Claim 42

This claim depends from claim 38, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the test controlling logic is configured to selectively logically remove the target memory location from a pool of memory available to operating system instances without requiring an operating system instance to halt execution. The Office Action asserts that Long discloses this element. The Office Action relies on Long, col. 1, lines 47-51 to support this assertion. However, these lines describe actions associated with cache miss processing. The "invalidating" described in Long deals with the freshness of a cache value and a cache value replacement policy. It has nothing to do with making a memory location unavailable to operating system instances. Additionally, to the extent that cache reconfiguring might achieve the claimed limitation, which is unlikely, the reconfiguring would require blocking an operating system instance from making an access to the memory location in question while the reconfiguring occurred. For these additional reasons this claim is not obvious and is in condition for allowance.

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Claim 43

This claim depends from claim 42, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the test controlling logic is configured to selectively logically remove the target memory location from a pool of memory by reprogramming the programmable memory address resolving logic. The Office Action asserts that Long discloses this element. The Office Action relies on Long, col. 1, lines 47-51 to support this assertion. However, these lines describe actions associated with cache miss processing and not with logically removing a memory location from a pool of memory. After the cache miss processing described in Long, the cache line in question would still be available. After the replacement processing in the claim, the memory location would no longer be available. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 44

Claim 44 has been amended to include the additional limitation that the "test memory location" and the "mirroring memory location" are less than a page of memory. Support for these limitations appeared in original paragraphs [0072] and [0073], which have also been amended to remove page sized operations. Since McKenzie only discloses page sized actions, claim 44 is not obvious and is in condition for allowance.

Claims 35-36 were rejected under 35 U.S.C. 103(a) as being unpatentable over Long, in view of McKenzie, and further in view of Korhonen.

Claim 35

Claim 35 has been amended to include the additional limitation that the "first memory location" and the "second memory location" are less than a page of memory. Support for these limitations appeared in original paragraphs [0072] and [0073], which have also been amended to remove page sized operations. Since McKenzie only discloses page sized actions, claim 35 is not obvious and is in condition for allowance.

Additionally, claim 35 concerns a computer-readable medium that stores processor executable instruction operable to perform a method that includes selecting, copying, logically

replacing, and initiating testing. The Office Action asserts that Korhonen "discloses a method using a test pattern for testing a memory page of a computer system while an operating system is active (col. 3, lines 13-15), where one or more software instructions for storing a pattern (col. 3, lines 40-41) may, ... be stored on a computer-readable medium". This assertion is inaccurate. What Korhonen discloses is a "system" that "includes software code" associated with storing a test pattern. A system is not a computer-readable medium. Even if it was, the only thing stored is a test pattern, not computer-executable instructions to do the claimed testing. For this additional reason this claim is not obvious and is in condition for allowance.

Note also that three references have been cobbled together to create this rejection. This feels like "hindsight reconstruction", which will be commented on later.

Claims 26-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Long, McKenzie, Leung, and Nakamura.

Claim 26

Claim 26 depends from claim 17, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that testing the first memory location includes two or more test methods. The Office Action asserts that the Nakamura abstract teaches a built-in self-test circuit for a memory including a test mode controller. The Office Action also asserts that Nakamura (col. 1, lines 15-18) teaches a microprocessor for generating different test patterns. This assertion is incomplete. What the passage in Nakamura really describes is how an "external memory tester ... includes a microprocessor for generating test patterns ... including column bars, checker board, marching, ..." While it is interesting that an external tester can produce different patterns, this clearly does not disclose the actual testing of a memory location using two or more test methods. While multiple patterns may be available to test using an external tester, Nakamura does not describe testing that includes multiple test methods applied to a single location.

Note also that four references have been pieced together to create this rejection. This feels like "hindsight reconstruction", which will be commented on later.

Claims 2 and 40 were rejected under 35 U.S.C. 103(a) as being unpatentable over Long, in view of McKenzie, and further in view of Idleman.

Claim 2

Claim 2 depends from claim 1, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, claim 2 recites that the memory mapping logic includes a crossbar. The Office Action asserts that Idleman (col. 4, lines 13-16) teaches the claimed crossbar. This is simply wrong. The reference describes how disk drive controllers, data disk drives, and error correction code disk drives can be connected using a crossbar. Clearly the crossbar that connects these devices is not located in a memory mapping logic. Similarly, Idleman describes how error correction circuitry can be connected to all of the buffer memory/disk drive data paths through crossbars. Once again this crossbar can not possibly be located in a memory mapping logic and yet connect the devices listed. For this additional reason this claim is not obvious and is in condition for allowance.

Note also that three references have been cobbled together to create this rejection. This feels like "hindsight reconstruction", which will be commented on later. This rejection illustrates the danger of keyword based searching to piece together three references. The "crossbar" found in by keyword search in Idleman is unrelated to the crossbar claimed to be a part of the memory mapping logic.

Claim 40

Claim 40 depends from claim 38, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, claim 40 has been amended to remove the address translation table, leaving only a crossbar. The Office Action asserts that Idleman (col. 4, lines 13-16) teaches the claimed crossbar. As described above this is simply wrong. The reference describes how devices can be connected using a crossbar. The device connecting crossbar can not possibly be located in a programmable memory address resolving logic.

Claims 4, 20 and 39 were rejected under 35 U.S.C. 103(a) as being unpatentable over four references: Long, McKenzie, Leung, and Chauvel.

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Claim 4

Claim 4 depends from claim 1, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites that the memory quality assurance logic can select the first memory location using a variety of methods. The Office Action asserts that Chauvel (par. 0018) discloses a method for managing memory in which replacement algorithms may include random replacement, round robin replacement, and least recently used replacement. While this may be true, it is irrelevant to this claim. This claim concerns how a location is selected to be tested. Chauvel concerns how memory management occurs. If Long, McKenzie, Leung, and Chauvel were combined, the combination would still not teach selecting a location to test based on one of the claimed methods. It is unlikely that the four references could even be combined, given the four separate technologies involved. But, even if they were, the combination would still not provide any mechanism for selecting the first memory location. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 20

Claim 20 depends from claim 17, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, claim 20 recites identifying the first memory location using one of a variety of methods. The Office Action asserts that Chauvel (par. 0018) discloses a method for managing memory in which replacement algorithms may include random replacement, round robin replacement, and least recently used replacement. While this may be true, it is irrelevant to this claim. This claim concerns how a location is selected to be tested. Chauvel concerns how virtual memory swapping occurs. If Long, McKenzie, Leung, and Chauvel were combined, the combination would still not teach selecting a location to test based on one of the claimed methods. The combination would teach a page level testing system whose memory management was performed by the described methods but whose pages were selected for testing by some unknown mechanism. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 39

This claim depends from claim 38, which has been shown to be not obvious, and thus this claim is similarly not obvious. Additionally, this claim recites identifying the target memory

location using one of a variety of methods. The Office Action asserts that Chauvel (par. 0018) discloses a method for managing memory in which replacement algorithms may include random replacement, round robin replacement, and least recently used replacement. As shown above, this is irrelevant to this claim. This claim concerns how a location is selected to be tested. Chauvel concerns how replacement of a virtual memory location occurs. Determining how to swap virtual memory locations is irrelevant to determining how to pick a memory location to test. For this additional reason this claim is not obvious and is in condition for allowance.

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Hindsight Reconstruction

Applicant will now comment on the propriety of combining three and four references in the manner performed in the Office Action. This appears to be hindsight reconstruction where the Office Action is using the Application as a blueprint to find parts of the claimed invention in unrelated references. Hindsight reconstruction has long been frowned upon:

> A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without **hindsight reconstruction** of the invention from the prior art. In making this evaluation, all facts must be considered. The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not, because it may doubt that the invention is patentable, resort to speculation, unfounded assumptions or **hindsight reconstruction** to supply deficiencies in its factual basis. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968) (emphases in original).

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). MPEP 2143.01

Here, the type of hindsight reconstruction engaged in by the Office Action is clearly impermissible. For example, keyword based hindsight reconstruction has clearly been applied for the "crossbar" rejections. While a reference (Idleman) was located that included the term "crossbar", the crossbar disclosed in the reference is irrelevant to the claimed crossbar. The crossbar in the reference is used to connect disk drives and other devices. The claimed crossbar is part of a memory mapping logic. These are very different crossbars. Thus, for at least the Idleman reference, the mere fact that references can be combined does not render the combination obvious, especially when the combination does not include the type of crossbar claimed.

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Conclusion

For the reasons set forth above, an early allowance of all claims is earnestly solicited.

Respectfully submitted,

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